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Implementation of Dormand-Prince based chaotic oscillator designs in different IQ-Math number standards on FPGA

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Abstract

Chaos and chaotic systems, one of the most important work areas in recent years, are used in areas such as cryptology and secure communication, industrial control, artificial neural networks, random number generators and image processing. The most basic structure used in these studies is a chaotic oscillator design that produces a chaotic signal. Chaotic oscillators are expressed by using differential equations. Numerical algorithms such as Euler, Heun, fourth order Runge-Kutta-4 (RK4), fifth order RK5-Butcher and Dormand-Prince are used for solving these differential equations. When the current literature is searched, chaotic oscillator designs are found by Euler, Heun, RK4 and RK5- Butcher method. However, FPGA-based chaotic oscillator design studies have not been found using the Dormand-Prince method, which produces more accurate solutions than other methods. In this work, self-excited attractor chaotic system was first designed in 16I-16Q, 14I-14Q, 12I-12Q, 10I_10Q, 8I-8Q IQ-Math number standards on FPGA using Dormand-Prince numerical algorithm and encoded in VHDL language. Xilinx ISE Design Tools were used to design the chaotic system. The design was synthesized and tested for the Xilinx Virtex-6 FPGA chip. Using the Xilinx ISE design tool, the chip statistics and maximum operating frequency obtained after the "Route-Place" operation are presented. In future work, safe communication and real random number generator applications can be realized by using the Dormand-Prince based oscillator design presented in this study.

Keywords: Dormand-Prince algorithm, FPGA, chaotic oscillator, VHDL.

1. INTRODUCTION

This Chaos and chaotic systems are one of the working areas on which many national and international studies have been conducted in the recent years. Chaotic systems, for the first time, were discovered by the mathematician and meteorologist Edward Norton Lorenz in 1963. Lorenz has revealed in his study that even the smallest change in initial conditions can cause unpredictable results after a while. The foundations of chaotic systems were laid with this study [1]. Then Sprott, Rössler, Rikitake, Burke-Shaw, Pehlivan-Wei, Abooee and Deng have proposed chaotic systems to the literature. Chaos and chaotic systems are those that are very tied to initial conditions, demonstrate random, nonlinear, disorganized looking forms but have a unique layout system in itself. These systems are

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variable and non-periodic structures producing noise-like signs. Chaotic systems are composed of simple differential equations even if they seem like complex structures [2]. A lot of research have been done in many research areas thanks to these properties of chaotic systems. These research areas include such fields as control [3, 4], image processing [5, 6], cryptology and secure communication [7, 8], artificial neural networks [9, 10], biomedical [11], industrial control [12, 13], and random number generators [14, 15]. In the literature, chaotic signal generators can be designed in different platforms. As an example of these platforms, digital signal processors (DSP) for the chaotic signal processor and chaotic communication systems was designed as a software-based and hardware-based by Dmitriev et al. [16]. Akgül et al., in their study, have carried out electronic circuit implementation of non-equilibrium point chaotic system, and produced phase portraits and oscilloscope outputs. This chaotic system has been made with LabVIEW based Field Programmable Gate Array (FPGA) chip and 32-bit floating-point number standard as FPGA based chaotic oscillator design. Then the results of FPGA-based design and LabVIEW-based design have been compared [17]. In the study of Pehlivan et al., chaotic oscillator design has been implemented for synchronization and masking communication circuits by using Matlab-Simulink and Orcad-PSpice programs with Rucklidge chaotic generator [18]. Rajagopalan et al., in their study, have stated that real random number generators can be used in secure communication thanks to their importance for cryptographic communication. It is also indicated in this study that in compliance with CMOS (Complementary Metal Oxide Semiconductor) Boolean chaotic generator, real random number generator design has been modeled using the Cadence virtuoso tool based on the 45 nm CMOS technology with ASIC (Application Integrated Circuit) approach [19]. In the study of Ge et al., they have proved Lyapunov asymptotic stability and worked on a Quantum-CNN (Cellular Neural Network) oscillator design of a special type of generalized synchronization of different order systems synchronized with three different layouts [20]. Chiuab et al., in their study, have implemented microprocessor based design of Lorenz chaotic system [21]. Tuna et al, in their study, have designed three dimensional chaotic core as FPGA chip as discrete-time by using Heun algorithm with 32-bit IQ-Math fixed-point number standard [22]. Koyuncu et al., in their study, have designed analog circuit model in PSpice program and digital integrated circuit model on FPGA chip using VHDL (Very High Speed Integrated Circuit Hardware Description Language) language and fourth order Runge-Kutta method and Sundarapandian-Pehlivan chaotic system. The results of the study have been compared [23]. By using Euler numerical algorithm, Azzaz et al., in their study, have implemented tree dimensional chaotic system with 32-bit (16Q-16I) fixed-point number format on Xilinx Virtex-II FPGA chip with VHDL language. The operation frequency of the design is specified as 38.86 MHz [24]. A chaotic signal generator generating chaotic signal is the most basic structure which is requisite for all these studies. Chaotic oscillators are expressed by using differential equations and these equations can be modeled with different numerical algorithms. Euler [25], Heun [26], the fourth order Runge Kutta (RK4) [27], and fifth order Runge Kutta Butcher (RK5-Butcher) [28] can be given as an example.

In this study, unlike from the before mentioned methods, the self-excited attractor (SEA) chaotic system is modeled using Dormand-Prince (DP) method for the first time. There was not such study when current literature was searched. In the second part of this study, some information about DP numerical algorithm and SEA chaotic system are given. In the third part, FPGA chips are briefly mentioned. In the fourth chapter, DP-based chaotic system's model and chip statistics are presented on FPGA chip. In the last section, the results obtained from the study have been evaluated.

2. DORMAND-PRINCE NUMERICAL ALGORITHM AND SEA CHAOTIC SYSTEM

In the literature, chaotic systems can be modeled using numerical algorithms like Euler, Heun, fourth order Runge-Kutta and fifth order Runge-Kutta-Butcher. The chaotic system presented in this study has been modeled using DP method for the first time. DP algorithm is given in equation (1). DP algorithm consists of seven steps of *k1, k2, k3, k4, k5, k6* and *k7.* In order to calculate the value of the algorithm, seven steps must be already calculated. Here, *k1* is the result obtained from initial conditions and h step number, *k2* value is the result obtained from h step number *and k1* value, *k3* value is the result obtained from h step number, *k1, and k2* values, *k4* value is the result obtained from h step number, *k1, k2, and k3* values, *k5* value is the result obtained from h step number, *k1, k2, k3, and k4* values, *k6* value is the result obtained from h step number, *k1, k2, k3, k4, and k5* values, *k7* value is the result obtained from h step number, *k1, k2, k3, k4 ,k5, and k6 values.* y_i value and *h* step number are used to calculate the next y_{i+1} value for numerical solution. In this equation, step interval of DP algorithm is taken as h=0.01 and the initial conditions $x_0=-1.8$, $y_0=-1.5$, $z_0=-2.5$ [29].

$$
\begin{aligned}
& y_{i+1} = y_i + h\left(\frac{35}{384}k_1 + \frac{500}{1113}k_3 + \frac{125}{192}k_4 - \frac{2187}{6784}k_5 + \frac{11}{84}k_6\right) \\
& k_1 = F(x_i, y_i) \\
& k_2 = F\left(x_i + \frac{h}{5}, y_i + \frac{h}{5}k_1\right) \\
& k_3 = F\left(x_i + \frac{3}{10}h, \left(y_i + \frac{3}{40}k_1 + \frac{9}{40}k_2\right)*h\right) \\
& k_4 = F\left(x_i + \frac{4}{5}h, \left(y_i + \frac{44}{45}k_1 - \frac{56}{15}k_2 + \frac{32}{9}k_3\right)*h\right) \\
& k_5 = F\left(x_i + \frac{8}{9}*h, \left(y_i + \frac{19372}{6561}k_1 - \frac{25360}{2187}k_2 + \frac{64448}{6561}k_3 - \frac{212}{729}k_4\right)*h\right) \\
& k_6 = F\left(x_i + 1*h, \left(y_i + \frac{9017}{3168}k_1 - \frac{355}{33}k_2 + \frac{46732}{5247}k_3 + \frac{49}{176}k_4 - \frac{5103}{18656}k_5\right)*h\right) \\
& k_7 = F\left(x_i + 1*h, \left(y_i + \frac{35}{384}k_1 + 0*k_2 + \frac{500}{1113}k_3 + \frac{125}{192}k_4 - \frac{2187}{6784}k_5 + \frac{11}{84}k_6\right)*h\right)
\end{aligned}
\tag{1}
$$

The mathematical expression of the chaotic system, expressed in the form of differential equations, is given in equation (2). Here, x, y, and z refer to the state variables of chaotic system, a, b, c, d, e, f and g refer to system parameters, and x_0, y_0, and z_0 refer to initial conditions. The values of parameters and initial conditions of submitted chaotic system are represented in equation (3).

$$
\begin{aligned}
& dx/dt = gz \\
& dy/dt = dx^2 + ey^2 - f \\
& dz/dt = -ax - bx^2 + cy^2
\end{aligned}
\tag{2}
$$

$$
\begin{aligned}
& a = f = 4, b = c = d = e = g = 1, \\
& x_0 = -1.8,\ y_0 = -1.5,\ z_0 = -2.5
\end{aligned}
\tag{3}
$$

Xu et al. has presented a new chaotic system with a self-excited attractor (SEA) to literature. In the study, they have introduced that is used for an engineering application of the signal encryption. In addition, a random number generator application has been performed using real circuit of SEA chaotic system. Parameter estimation procedure is based on the attractor distribution modeling in the state space. The results of presented study show the success of the parameter estimation method [30]. The selected chaotic system was first modeled as Matlab-based. In consequence of Matlab analysis, time series are presented in Figure 1 and phase portraits are presented in Figure 2.

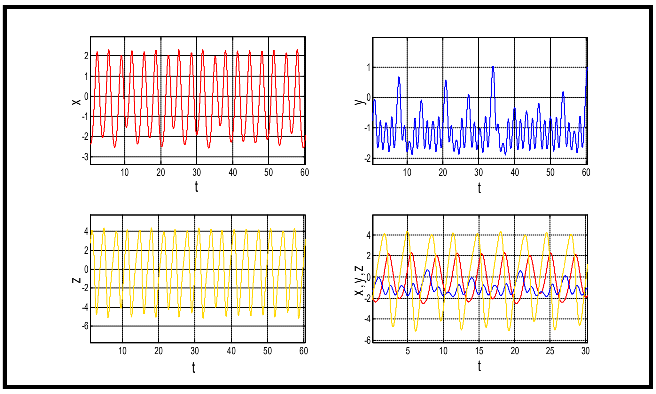

Figure 1. DP-based SEA chaotic oscillator time series

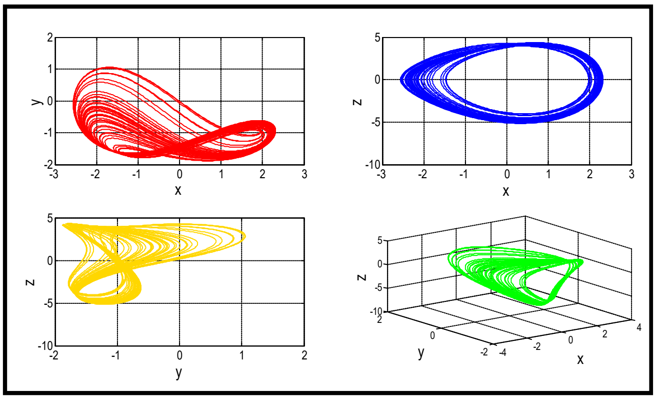

Figure 2. DP-based SEA chaotic oscillator phase series

The analysis of time series of the chaotic system's y variable belonging to Heun, RK-4, RK5B, and DP is presented in Fig. 3. DP method produces more accurate results compared to other algorithms [31, 32]. Furthermore, since the previous value is used to calculate the next step of the system, it is seen that the difference between DP and other algorithms is increasing.

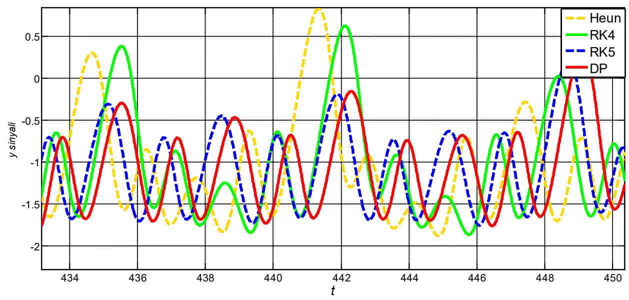

Figure 3. Time series of Heun, RK-4, RK5-Butcher and DP algorithms for the SEA chaotic system.

3. FPGA CHIPS

FPGA chips are digital integrated circuits that can be programmed in the field repeatedly, producing the hardware structure according to the logical function required by the designer. Interconnections, logical blocks, and input/output blocks can be programmed in the field in compliance with the logical circuit that the designer makes. According to the logical circuit the designer makes, interconnections, logical blocks and input / output blocks can be programmed in the field. FPGA chips have gained popularity due to their real-time, high-frequency, and parallel processing capability and even the ability to take processor into them. Recently, there are FPGA chips starting from a few MHz and operating frequency up to a few GHz. Another advantage of FPGA chips is that it allows the faster design of the desired design by using IP core (Intellectual Properties-core) structures. FPGA chips have three main structures, namely input-output blocks (I-O blocks), configurable logical blocks (CLB), and interconnection network [33, 34].

Input-Output Blocks; I/O blocks are programmable pins of *FPGA*. These pins can be programmed as input, output or both input and output according to the designer's request. I / O pins also allow external data to reach inside the chip. There are also many input output pins on the FPGA chip, such as power pins, clock pins, configuration pins and user pins [35].

Configurable Logic Blocks (CLB)); They consist of LUT (Look-up table) that is also called logic cell where logical functions are created, Flip-Flop where one bit of information is held, and Mux that manages information flow. LUTs are small memories that perform a logic process [36].

Interconnections; these connections have a flexible programmable structure. Their main task is to establish connections between logical blocks or to establish connections between logical blocks and input/output pins [37].

4. DORMAND-PRINCE-BASED CHAOTIC OSCILLATOR DESIGN ON FPGA

The chaotic system presented in this study was modeled to work on FPGA with IQ-Math fixed point number standard using DP numerical algorithm. The design was coded using VHDL language which is a hardware description language. The top level block diagram of this designed chaotic oscillator obtained by using Xilinx ISE 14.7 is shown in Fig. 4.

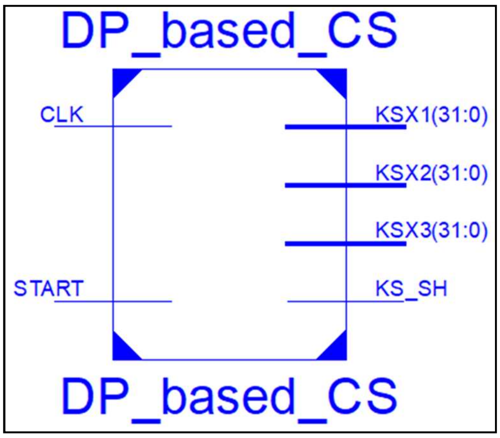

Figure 4. The top level block diagram of DP-based SEA chaotic system on FPGA

The 1-bit START signal on the designed chaotic system refers to the control signal required to operate the system and the 1-bit CLK signal refers to the synchronization signal of the system. At the system output, there are 1-bit KS_SH signal indicating the unit produces a result and KSX1, KSX2, and KSX3 signals carrying chaotic signal value. The second sub-block structure of the design consists of the most basic elements such as multiplexer unit (MUX), chaotic oscillator unit and filter unit as shown in Fig. 5.

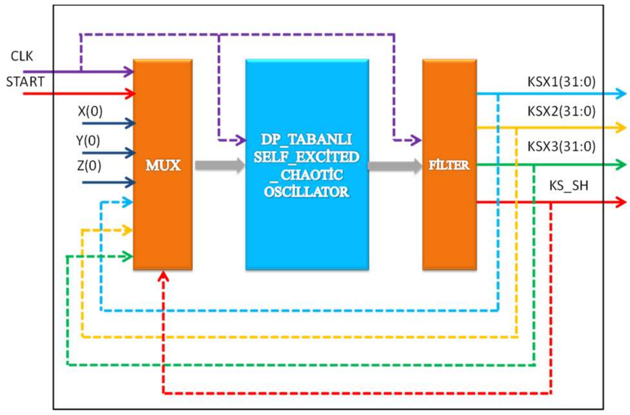

Figure 5. The second sub-level block diagram of FPGA-based chaotic oscillator

In this study, the design purpose of multiplexer unit is to take user-assigned initial conditions X(0), Y(0), Z(0) values at the first run and to take these values from filter output at the next stages. 1-bit KS_SH signal becomes '1' when the system produces the first result and the system sends this signal to the mux unit, allowing the results produced by the chaotic system to be used instead of the initial values that were originally assigned. The purpose of the filter is to design the chaotic oscillator to filter out unwanted signals. The purpose of DP-based SEA chaotic oscillator structure is to calculate the differential equations of chaotic system using DP numerical algorithm. Figure 6 shows the third level block diagram of DP-based SEA chaotic oscillator. The basic units used in the chaotic system, such as the multiplier, collector, divider and extraction, were created using the IP-Core Generator, which is compliant with the fixed-point number standards. This implemented chaotic oscillator was tested by creating test bench unit in VHDL language. Figure 7-11. shows the simulation results obtained by using Xilinx ISE Design Tools program of DP-based SEA chaotic system.

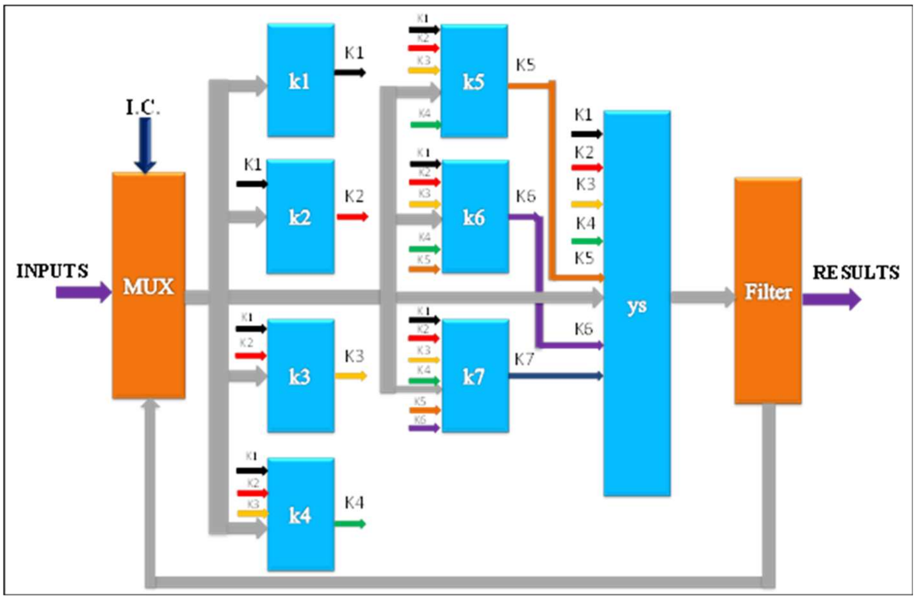

Figure 6. The third level block diagram of DP-based SEA chaotic oscillator

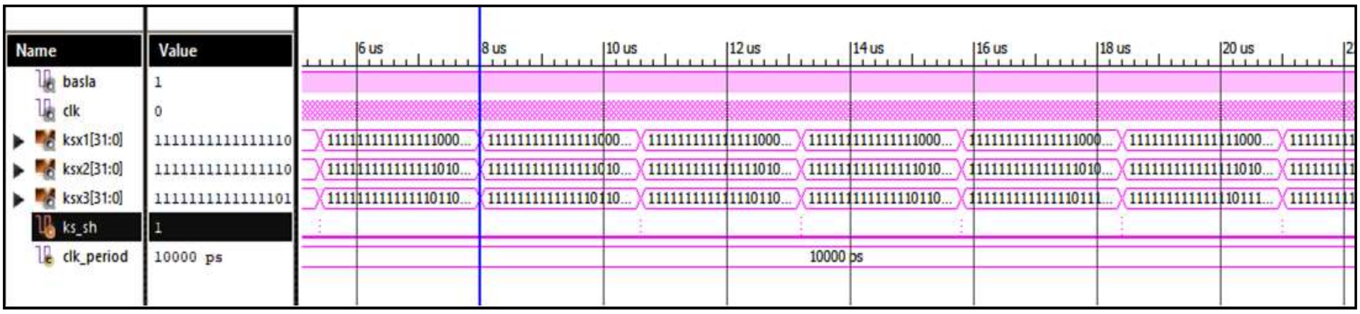

Figure 7. Simulation results of Xilinx ISE 14.7 of DP-based 16I-16Q fixed-point number standard SEA chaotic oscillator

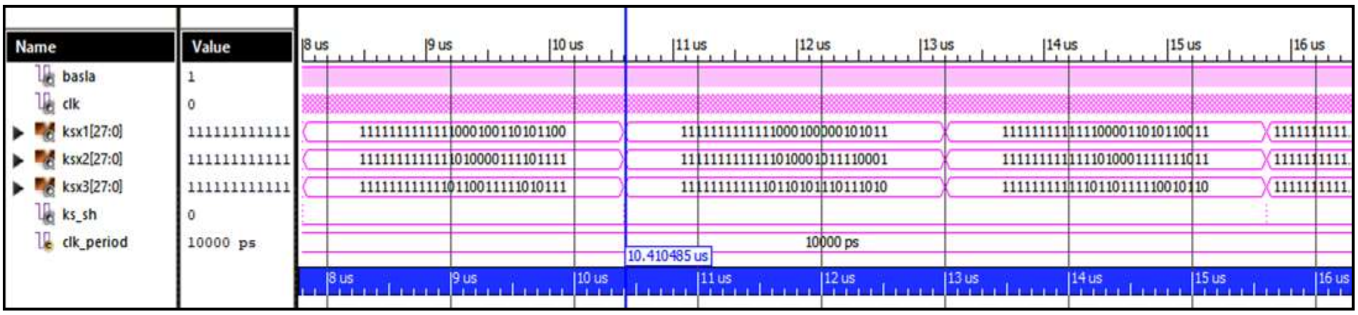

Figure 8. Simulation results of Xilinx ISE 14.7 of DP-based 14I-14Q fixed-point number standard SEA oscillator

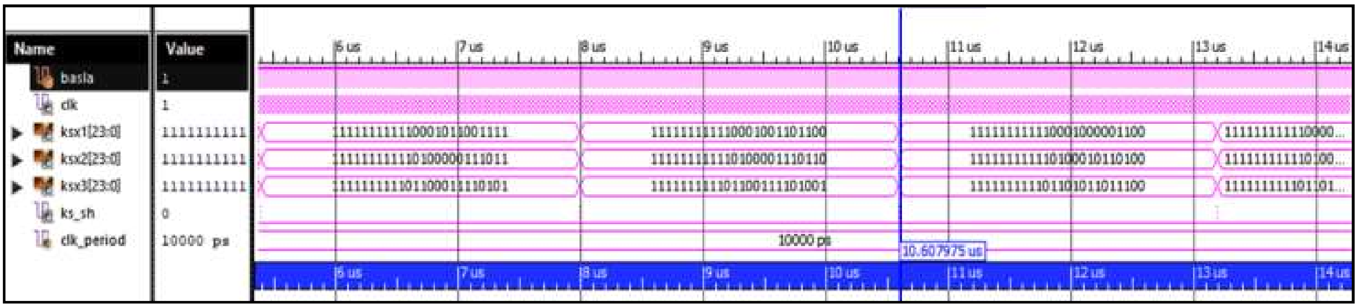

Figure 9. Simulation results of Xilinx ISE 14.7 of DP-based 12I-12Q fixed-point number standard SEA oscillator

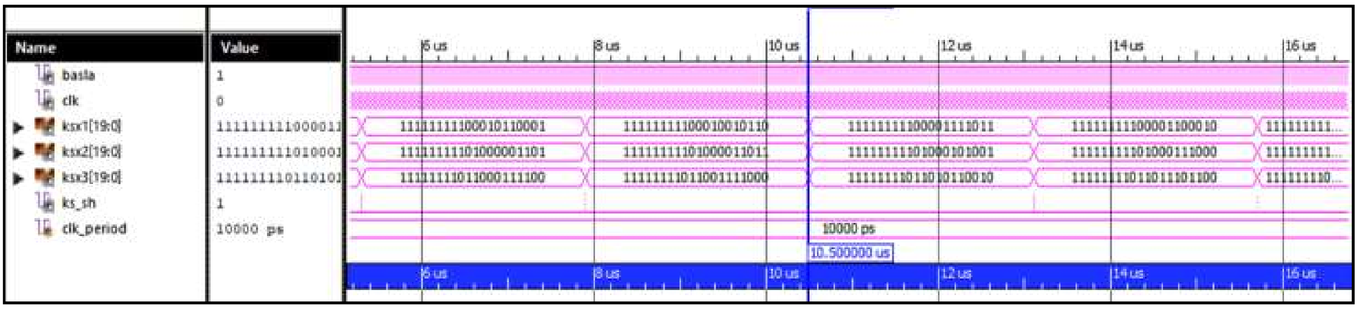

Figure 10. Simulation results of Xilinx ISE 14.7 of DP-based 10I-10Q fixed-point number standard SEA oscillator

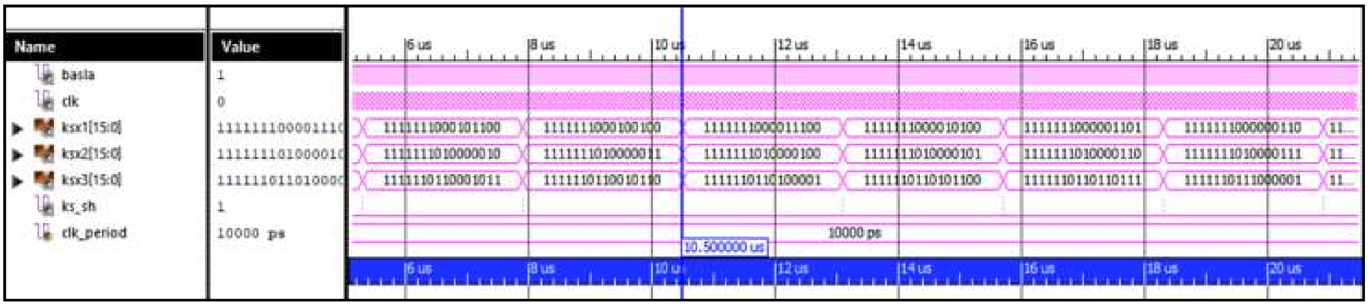

Figure 11. Simulation results of Xilinx ISE 14.7 of DP-based 8I-8Q fixed-point number standard SEA oscillator

SEA chaotic systems in the designed 16I-16Q, 14I-14Q, 12I-12Q, 10I-10Q, 8I-8Q IQ-Math number standards were tested by loading the XC6LVX240T chip of the Virtex-6 family of Xilinx, respectively. Then the chip statistics obtained after Place & Route operations are presented in table 1. Table 1 shows the use of chip hardware resources in different number standards. According to this table, the chaotic system in the 16I-16Q IQ-Math number standard used more chip hardware resources than the chaotic system in the 8I-8Q IQ-Math number standard. In addition, the chaotic system with the 8I-8Q number standard has the highest operating frequency. The lowest operating frequency was found to have the chaotic system of the 16I-16Q number standard. The design of the 16I-16Q, 14I-14Q, 12I-12Q, 10I-10Q, 8I-8Q IQ-Math number standards of the SEA chaotic systems produced by FPGA-based 3x100 data set has been recorded in the excel file. According to the recorded data, the system outputs of the chaos systems KSX1, KSX2 and KSX3 and the results of the Matlab-based chaotic system were analyzed for individual MSE and RMSE errors. As a result of these analyzes, the minimum error values for the SEA chaotic system are in the chaotic system of the 16I-16Q IQ-Math number standard and the highest error is in the chaotic system of the IQ-Math number standard 8I-8Q. Mean squared error (MSE) and root mean squared error (RMSE) error analyzes were made by comparing Matlab-based results with FPGA-based results and given in table 2.

Table 1. FPGA chip usage statistics of DP-based SEA chaotic system

Device Utilization Summary (estimated values)	16I-16Q Chaotic sis.	14I-14Q Chaotic sis.	12I-12Q Chaotic sis.	10I-10Q Chaotic sis.	8I-8Q Chaotic sis.
Number of Slice Registers	18280/ 301440 6%	16529/ 301440 5%	13888/ 301440 4%	11575/ 301440 3%	12747/ 301440 4%
Number of Slice LUTs	14473/ 150720 9%	13020/ 150720 8%	11773/ 150720 7%	10260/ 150720 6%	13550/ 150720 8%
Number used as Memory	7953/ 58400 13%	7247/ 58400 12%	6747/ 58400 11%	6144/ 58400 10%	10169/ 58400 17%
Number of BUFG/BUFGCTRLs	1/32 3%	1/32 3%	1/32 3%	1/32 3%	1/32 3%
Number of DSP48E1s	712/768 92%	712/768 92%	356/768 46%	356/768 46%	178/768 23%
Max. Operating Frequency (MHz)	344.585 MHz	349.599 MHz	354.762 MHz	360.080 MHz	365.559 MHz

Table 2. MSE ve RMSE error analysis DP-based SEA chaotic oscillator

IQ-Math Fixed point	OUTPUT	MSE	RMSE
16I-16Q	X	1,23E-05	3,52E-03
	Y	7,08E-06	2,66E-03
	Z	1,75E-05	4,19E-03
14I-14Q	X	2,82E-04	1,68E-02
	Y	1,38E-04	1,17E-02
	Z	5,99E-04	2,45E-02
12I-12Q	X	4,38E-03	6,62E-02
	Y	1,90E-03	4,36E-02
	Z	1,04E-02	1,02E-01
10I-10Q	X	4,93E-02	2,22E-01
	Y	3,94E-02	1,99E-01
	Z	6,24E-02	2,50E-01
8I-8Q	X	8,79E-01	9,38E-01
	Y	4,60E-01	6,78E-01
	Z	1,7756069	1,33252

5. RESULTS AND DISCUSSIONS

A chaotic oscillator structure producing chaotic signal is the most basic structure used in chaos-based applications such as cryptology, secure communications, industrial control, artificial neural networks, random number generators, and image processing. Because chaotic systems are expressed by differential equations, Euler, Heun, fourth order Runge-Kutta and fifth order Runge-Kutta-Butcher based solutions have been proposed for numerical solutions of chaotic systems in the literature. In this study, unlike the numerical methods presented in the literature, SEA chaotic system has been designed on FPGA with IQ-Math fixed-point number standard using DP numerical algorithm. The operating frequencies of chaotic oscillator designs were obtained between 344.585 MHz and 365.559 MHz. The design has been coded in VHDL language by using Xilinx ISE Design Tools. It has been synthesized and tested for Xilinx Virtex-6 FPGA chip. In future work, safe communication and real random number generator applications can be realized by using the DP-based oscillator design presented in this study.

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REFERENCES

[1] Tuna, M., Fidan, C.B., "A Study on the importance of chaotic oscillators based on FPGA for true random number generating (TRNG) and chaotic systems", *Journal of the Faculty of Engineering and Architecture of Gazi University*, 33(2), pp: 469-486, 2018.

[2] Yılmaz D., Güler N.F., A Study on the Chaotic Time Series Analysis, *Journal of the Faculty of Engineering and Architecture of Gazi University*, 21 (4), 759-779, 2006.

[3] Yassen, M. T., Chaos synchronization between two different chaotic systems using active control," *Chaos, Solitons & Fractals*, *23*(1): 131-140, 2005.

[4] Park, J. H., and Kwon, O. M., "A novel criterion for delayed feedback control of time-delay chaotic systems". *Chaos, Solitons & Fractals*, 23.2: 495-501, 2005.

[5] Chen, G., Mao, Y., & Chui, C. K. "A symmetric image encryption scheme based on 3D chaotic cat maps", *Chaos, Solitons & Fractals, 21*(3), 749-761, 2004.

[6] Pareek, Narendra K., Vinod, Patidar, and Krishan, K. Sud. "Image encryption using chaotic logistic map", *Image and vision computing,* 24: 9926-934, 2006.

[7] Pehlivan, İ., Uyaroğlu, Y., Yalçın, M. A., & Ferikoğlu, A. "Sprott_94_A Kaotik Sisteminin Senkronizasyonu ve Bilgi Gizlemede Kullanılması," *Uluslararası Katılımlı Bilgi güvenliği ve Kriptoloji Konferansı*, 2007.

[8] Çavuşoğlu, Ü., Zengin, A., Pehlivan, I., & Kaçar, S. (2017). A novel approach for strong S-Box generation algorithm design based on chaotic scaled Zhongtang system. *Nonlinear Dynamics*, *87*(2), 1081-1094.

[9] Alçın, M., "The Effect on Modelling Performance of Different Activation Functions for Feed Forward and Feedback Network Structures in Modeling of Chen Chaotic System," *International Journal of Scientific and Technological Research*, ISSN 2422-8702 (Online), Vol 3, No.7, 2017.

[10] Karunasinghe, Dulakshi SK, and Shie-Yui Liong., "Chaotic time series prediction with a global model: Artificial neural network," *Journal of Hydrology,* 323.1-4: 92-105, 2006.

[11] Lin, J. S., & Huang, S. M. "An FPGA-based brain-computer interface for wireless electric wheelchairs," *In Applied Mechanics and Materials*, (Vol. 284, pp. 1616-1621). Trans Tech Publications, 2013.

[12] dos Santos C.L., "Tuning of PID controller for an automatic regulator voltage system using chaotic optimization approach," *Chaos, Solitons & Fractals, 39*(4): 1504-1514, 2009.

[13] Lu, J., Xinghuo Y., and Guanrong C., "Generating chaotic attractors with multiple merged basins of attraction: A switching piecewise-linear control approach*," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 50.2: 198-207, 2003.

[14] Kaçar, S. (2016). Analog circuit and microcontroller based RNG application of a new easy realizable 4D chaotic system. *Optik*, *127*(20), 9551-9561.

[15] Çavuşoğlu, Ü., Kaçar, S., Pehlivan, I., & Zengin, A. (2017). Secure image encryption algorithm design using a novel chaos based S-Box. *Chaos, Solitons & Fractals*, *95*, 92-101.

[16] Dmitriev, A., Starkov, S., and Yemetz, S., "Chaotic communication using digital signal processors," *Nonlinear Theory and Applications,* 3: 1093-1096, 2000.

[17] Alçın, M., Tuna, M., Koyuncu, İ., "IQ-Math Based Designing of Fourth Order Runge-Kutta Algorithm on FPGA and Performance Analysis

According to ANN Approximation," *International Journal of AdvancedResearch in Science Engineering and Technology,* 5(8): 6523–6530, 2018.

[18] Pehlivan, İ., Uyaroğlu, Y. ve Yoğun, M., "Chaotic oscillator design and realizations of the Rucklidge attractor and its synchronization and masking simulations," *Scientific Research and Essays,* 5(16): 2210-2219, 2010.

[19] Rajagopalan, S., Rethinam, S., Deepika, A. N., Priyadarshini, A., Jyothirmai, M., Rengarajan, A., Rajagopalan, Sundararaman, et al. "Design of boolean chaotic oscillator using CMOS technology for true random number generation," *Microelectronic Devices, Circuits and Systems (ICMDCS),* International conference on: 1-6, 2017.

[20] Ge, Z. M. ve Yang, C. H., "The generalized synchronization of a Quantum-CNN chaotic oscillator with different order system," *Chaos, Solitons and Fractals,* 35: 980–990, 2008.

[21] Chiuab, R., Gonzaleza, M. M., Mancillaa, D. L., "Implementation of a Chaotic Oscillator into a Simple Microcontroller*," IERI Procedia* 4: 247–252, 2013.

[22] Tuna, M., Fidan, C. B., Koyuncu, İ., & Pehlivan, İ., "Real time hardware implementation of the 3D chaotic oscillator which having golden-section equilibra," *24th IEEE In Signal Processing and Communication Application Conference (SIU),* pp. 1309-1312, 2016.

[23] Alcin, M., Koyuncu, I., Tuna, M., Varan, M., & Pehlivan, I., "A novel high speed Artificial Neural Network–based chaotic True Random Number Generator on Field Programmable Gate Array," *International Journal of Circuit Theory and Applications*, 47(3), 365-398, 2019.

[24] Azzaz, M.S., Taugast, C., Sadoudi, S., Fellah, R., Dandache, A., "A new auto-switched chaotic system and its FPGA implementation," *Communications in Nonlinear Science and Numerical Simulation,* 18 (7), 1792-1804, 2013.

[25] Lee, S. H., Kapila, V., Porfiri, M., & Panda, A., "Master–slave synchronization of continuously and intermittently coupled sampled-data chaotic oscillators," *Communications in Nonlinear Science and Numerical Simulation, 15*(12), 4100-4113, 2010.

[26] Tuna, M., & Fidan, C. B. "Electronic circuit design, implementation and FPGA-based realization of a new 3D chaotic system with single equilibrium point," *Optik-International Journal for Light and Electron Optics, 127*(24), 11786-11799, 2016.

[27] Tlelo-Cuautle, E., Rangel-Magdaleno, J. J., Pano-Azucena, A. D., Obeso-Rodelo, P. J., & Nuñez-Perez, J. C. "FPGA realization of multi-scroll chaotic oscillators," *Communications in Nonlinear Science and Numerical Simulation, 27*(1-3), 66-80, 2015.

[28] Koyuncu, İ., Şahin, İ., Gloster, C., & Sarıtekin, N. K. "A Neuron Library for Rapid Realization of Artificial Neural Networks on FPGA: A Case Study of Rössler Chaotic System," *Journal of Circuits, Systems and Computers,* 26(01), 1750015. 2017.

[29] Alçın, M., Pehlivan, İ., & Koyuncu, İ. "Hardware design and implementation of a novel ANN-based chaotic generator in FPGA," *Optik-International Journal for Light and Electron Optics*, *127*(13), 5500-5505, 2016.

[30] Xu, G., Shekofteh, Y., Akgül, A., Li, C., & Panahi, S., "A new chaotic system with a self-excited attractor: entropy measurement, signal encryption, and parameter estimation," Entropy, 20(2), 86, 2018.

[31] Tuna, M., Koyuncu, İ., & Alçın, M., "Fixed and floating point-based high-speed chaotic oscillator design with different numerical algorithms on FPGA, " *Int J Adv Res Electr Electron Instrum Eng*, 7(7), 3179-3187, 2018.

[32] Tuna, M., Alçın, M., Koyuncu, İ., Fidan, C. B., & Pehlivan, İ., "High Speed FPGA-based Chaotic Oscillator Design," *Microprocessors and Microsystems*, 66, 72-80, 2019.

[33] Jin, C., Herder, C., Ren, L., Nguyen, P. H., Fuller, B., Devadas, S., & van Dijk, M. "Fpga implementation of a cryptographically-secure puf based on learning parity with noise," *Cryptography, 1*(3), 23, 2017.

[34] Ratnayake, K., & Amer, A. "Embedded architecture for noise-adaptive video object detection using parameter-compressed background modeling," *Journal of Real-Time Image Processing, 13*(2), 397-414, 2017.

[35] Koyuncu I, "Implementation of High Speed Tangent Sigmoid Transfer Function Approximations for Artificial Neural Network Applications on FPGA," *Advances in Electrical and Computer Engineering,* 18, 79–86, 2018.

[36] Rajagopal, K., Guessas, L., Vaidyanathan, S., Karthikeyan, A., & Srinivasan, A. "Dynamical analysis and FPGA implementation of a novel hyperchaotic system and its synchronization using adaptive sliding mode control and genetically optimized PID control," *Mathematical Problems in Engineering,* 2017.

[37] Chinna, S., Dharmar, S., & Shanmugavel, K. L. "Hardware Implementation of Road Network Extraction Using Simplified Gabor Wavelet in Field Programmable Gate Array," *International Journal of Engineering and Technology Innovation*, *8*(3), 200-216, 2018.